

List of Figures and Tables

Table 1.1	Decimal, binary and hexadecimal notations of the integers 0, 1, ..., 15	12
Figure 1.2	Representation of information	12
Figure 1.3	Comparison of analog and digital computation	13
Figure 1.4	Structure of the hybrid computer	13
Figure 1.5	Von Neumann structure of computer	14
Figure 1.6	Bus oriented computer	16
Figure 1.7	Bus oriented multiprocessor computer	17
Figure 1.8	Structure and function of three-address instruction	17
Figure 1.9	Structure and function of two-address instruction	18
Figure 1.10	Structure and function of one-address instruction	18
Figure 1.11	Address types	19
Figure 1.12	Two ways of mapping operands into memory bytes	21
Table 1.13	Machine and assembly language comparison	22
Figure 1.14	Memory linear organization	22
Table 2.1	Inner registers of the 8086	24
Table 2.2	Structure of the 8086's flag register	24
Figure 2.3	Use of segment registers in the 8086	26
Figure 2.4	Evaluating absolute address in the 8086	26
Figure 2.5	Illustration of PUSH and POP operations	33
Figure 2.6	Effects of shifts and rotations	40
Figure 2.7	Effect of conditional jumps	41
Figure 2.8	Effect of intersegment (or far) direct jump	45
Figure 2.9	Effects of the intrasegment indirect jumps:	46
Figure 2.10	Effects of the intersegment indirect jumps	46
Figure 2.11	Effect of the near call and the near return from the subroutine	50
Figure 2.12	Effect of the far call and the far return from the subroutine	50
Figure 2.13	Example of machine instruction using immediate addressing	53
Figure 2.14	Example of machine instruction using register addressing mode	54
Figure 2.15	Example of machine instruction using direct addressing mode	54
Figure 2.16	Example of machine instruction using register indirect addressing mode	55
Figure 2.17	Example of machine instruction using indexed addressing:	56
Figure 2.18	Example of machine instruction using based addressing mode	57
Figure 2.19	Example of machine instruction using indexed and based addressing mode	57
Figure 2.20	Program and interrupt service routine	58
Figure 2.21	Interrupt vector table of the 8086	59
Figure 2.22	Effects of instructions STI, CLI and IRET	60
Figure 2.23	Simplified instruction cycle of the 8086	61
Figure 2.24	Interconnecting the microprocessor 8086 and the interrupt controller 8259A	62
Figure 3.1	General logical circuit	64
Table 3.2	Truth tables of some selected logical functions	65
Table 3.3	Boolean algebra laws	66

Table 3.4	Derived Boolean algebra laws	66
Figure 3.5	Maps	67
Table 3.6	Truth tables for half adder	68
Table 3.7	Truth table for full adder	68
Figure 3.8	One-bit adder	68
Figure 3.9	Maps for one-bit adder	69
Figure 3.10	Symbols of some logic elements	70
Figure 3.11	Implementation of half adder	70
Figure 3.12	Symbols for decoder, multiplexer and demultiplexer	70
Figure 3.13	Implementation of multiplexer and demultiplexer	71
Table 3.14	Tables for decoder from Fig. 3.12.a	71
Table 3.15	Expressions for decoder from Fig. 3.12.a	71
Table 3.16	Truth table for multiplexer from Fig. 3.12.b	72
Table 3.17	Tables for demultiplexer 4×1	73
Table 3.18	Expressions for demultiplexer 4×1	73
Figure 3.19	Interconnecting computer units by bus	73
Figure 3.20	Standard output (totem-pole)	74
Figure 3.21	Tri-state output	75
Figure 3.22	Open collector	75
Figure 3.23	Standard structure of sequential logical circuit	76
Table 3.24	Computational steps within 8-bit serial adder	77
Figure 3.25	State diagram of serial adder	78
Table 3.26	State table and output table of the serial adder	79
Figure 3.27	State diagram of counter mod 3	79
Figure 3.28	State diagram of computer control unit	80
Figure 3.29	Combinational part of the serial adder	81
Figure 3.30	Serial adder	81
Figure 3.31	Timing of synchronous sequential circuit	82
Figure 3.32	Basic memory elements of type RS	83
Figure 3.33	Synchronous D flip-flop	84
Figure 3.34	Behavior of level sensitive and edge sensitive memory elements	85
Figure 3.35	Example of register inner structure	86
Figure 3.36	inner structure of simple circuit of type PLA	87
Table 4.1	The most frequently used radix q number systems	89
Figure 4.2	Addition and subtraction modulo \mathcal{M}	92
Table 4.3	Binary addition	93
Figure 4.4	Binary adder	93
Figure 4.5	Subtraction using binary adder	96
Figure 4.6	Add/subtract unit	96
Table 4.7	Example of biased code	97
Figure 4.8	Example of biased code	97
Figure 4.9	Biased code	97
Figure 4.10	Sign and magnitude representation	97
Table 4.11	Example of sign and magnitude code	98
Figure 4.12	Example of sign and magnitude code	98
Figure 4.13	Sign and magnitude code	98
Figure 4.14	Addition and subtraction for sign and magnitude representation	99
Figure 4.15	Some samples of the sign and magnitude addition	100
Table 4.16	Example of 2's complement code	102
Figure 4.17	Example of 2's complement code	102

Figure 4.18	2's complement code	102
Table 4.19	2's complement addition	102
Figure 4.20	2's complement addition	102
Figure 4.21	Some samples of 2's complement addition	103
Figure 4.22	2's complement addition	103
Figure 4.23	2's complement adder	104
Figure 4.24	Some samples of 2's complement subtraction	105
Figure 4.25	Add/subtract unit for both unsigned numbers and 2's complement code	105
Table 4.26	Some 4-bit decimal codes	106
Figure 4.27	Decimal adder (the parallel one)	107
Figure 4.28	One-position decimal adder for BCD code	108
Table 4.29	An example of 10's complement code	111
Figure 4.30	Shifters — logical	113
Figure 4.31	Shifters — cyclic	114
Figure 4.32	Shifters — arithmetic — sign and magnitude	115
Table 4.33	Binary addition for $a_i = b_i$	115
Figure 4.34	Shifters — arithmetic — 2's complement	115
Figure 4.35	Sign extension	116
Figure 4.36	Binary multiplication — I.	118
Figure 4.37	Binary multiplication — II.	118
Figure 4.38	Binary multiplier	118
Figure 4.39	Restoring binary division	125
Figure 4.40	Nonrestoring binary division	125
Figure 4.41	Implementation of nonrestoring binary division	127
Figure 4.42	Floating-point format after US Air Force MIL-STD-1750A	128
Figure 4.43	floating-point format after ANSI/IEEE Std 754-1985	132
Table 4.44	Part of ASCII code	134
Table 4.45	Czech letters coding	135
Figure 5.1	Inner structure of memory chip	140
Figure 5.2	Memory read cycle	141
Figure 5.3	Memory write cycle	141
Figure 5.4	Interfacing memory chip	142
Figure 5.5	Mapping microprocessor address space for interfacing from Fig. 5.4	142
Figure 5.6	Examples of partially decoded microprocessor address space	143
Figure 5.7	Interfacing more memory chips to extend memory address space	144
Figure 5.8	Examples of mapping the CPU address space into memory address space	144
Figure 5.9	Interfacing memory chips to extend size of memory addressable unit	145
Figure 5.10	Inner structure of SRAM integrated chip	145
Figure 5.11	Comparison of SRAM cell and DRAM cell inner structure	147
Figure 5.12	Inner structure of DRAM integrated circuit	148
Figure 5.13	Principle of a magnetic read/write head	149
Figure 5.14	Various data encoding schemes	150
Figure 5.15	Arrangement of cylinders, tracks and sectors	151
Figure 5.16	Track and sector inner structure	152
Figure 5.17	Sector arrangement for case of sector interleaving coefficient $F_i=3$	154
Figure 5.18	Disk drive interconnection	155
Figure 5.19	Hierarchical memory system	156
Table 5.20	The access times of typical memories	157
Figure 5.21	Comparison of RAM and CAM memories	159
Figure 5.22	Principles used to implement cache memory	159

Figure 5.23	Principle of direct mapped cache	160
Figure 5.24	Principle of two-way set cache	161
Figure 5.25	Virtual address translation for segmentation	163
Figure 5.26	Principle of paging: mapping pages into frames	164
Figure 5.27	Virtual address translation for paging	164
Figure 6.1	Raster scan cathode ray tube	166
Figure 6.2	Example of character dot patterns	166
Figure 6.3	VIDEO RAM and character generator cooperation	167
Figure 7.1	Basic cycle of processor	173
Figure 7.2	Control unit	175
Figure 7.3	Instruction fetch	176
Figure 7.4	Arithmetic and logic operations	178
Figure 7.5	Jumps	178
Figure 7.6	Interrupt of HW service	178
Table 7.7	Some control and state signals	180
Figure 7.8	Instruction fetch — another form of flowchart	180
Figure 7.9	Instruction fetch — state diagram	180
Figure 7.10	Part of hard-wired controller	181
Figure 7.11	Structure of horizontal microinstruction	182
Figure 7.12	Horizontal-oriented microcontroller	183
Table 7.13	Fragment of microprogram	184
Figure 8.1	Client server cooperation	188
Figure 8.2	Spreading signal along a bus	189
Figure 8.3	Delayed retransmission after collision	190
Figure 8.4	Frame format used in Ethernet	191
Figure 8.5	Interconnecting PC to Ethernet cable	191
Figure 8.6	Token bus arrangement	192
Figure 8.7	Token ring arrangement	192
Figure 8.8	Possible modes of station interface in the token ring	193
Figure 8.9	Implementation of the token ring	193
Figure 8.10	Comparison of throughput dependence of LANs	194
Figure 8.11	Interconnecting net segments by means of repeaters	194
Figure 8.12	Use of bridges to interconnect LANs of different types	195
Figure 8.13	General structure of wide area network	196
Figure 8.14	Way of servicing frames inside gateway	197
Figure 8.15	Principle of stop and wait protocol	199
Figure 8.16	Simplified structure of the Internet	199