## Contents

1	Language			
	1.1	Prior Perceptions	1	
	1.2	A Spectrum of Digital Languages	3	
	1.3	Control Flow	6	
	1.4	Terms and Roles	8	
	1.5	Some Digital History	9	
2	Boolean Algebra and Digital Logic			
	2.1	Computer Logic Circuits	11	
	2.2	Application of Logic Circuits	15	
	2.3	Evaluation of Boolean Functions	19	
	2.4	Boolean Algebra	21	
	2.5	Simplification of Boolean Functions	26	
	2.6	Boolean Algebra as an Algebra of Subsets	28	
	2.7	On the History of the Algebra of Logic	31	
		Problems	31	
		References	33	
3	0,	1: Binary Numbers or Logical Values?	35	
	3.1	The Binary Number System	35	
	3.2	Conversion between Bases	37	

X	Contents

	3.3	Binary Coding of Decimal Digits	40	
	3.4	Historical Note	43	
		Problems	44	
		References	44	
4	Sin	nplification of Boolean Functions	45	
	4.1	Standard Forms of Boolean Functions	45	
	4.2	Karnaugh Map Representation of Boolean Functions	52	
	4.3	Simplification of Functions on the Karnaugh Map	60	
	4.4	Map Minimization of Product-of-Sums Expressions	66	
	4.5	Incompletely Specified Functions	68	
		Problems References	71	
		References	73	
5	Sta	ndard Digital Integrated Circuits	75	
	5.1	Introduction	75	
	5.2	Small-Scale Integrated Circuits	79	
	5.3	Fan-out, Fan-in, and Noise Immunity	80	
	5.4	Switching Delay in Logic Circuits	85	
	5.5 5.6	Circuit Implementation with NAND and NOR Gates Multilevel All-NAND Realizations	87	
	5.7	Reducing Package Counts in Multilevel Realizations	89 94	
	5.7	Problems	98	
		References	101	
6	Co	101		
	6.1	Introduction	102	
	6.2	Conversion between Number Bases	103 103	
	6.3	Coding of Information	106	
	6.4	Parity	111	
	6.5	Binary Arithmetic	113	
	6.6	Implementation of Binary and BCD Addition	117	
	6.7	Carry and Overflow	121	
		Problems	123	
		References	126	
7	Combinational MSI Parts, ROMs, and PLAs			
	7.1	Perspective	127	
	7.2	Combinational MSI Parts	128	
	7.3	Read-Only Memory	137	
	7.4	Chip-Select, Buses, and Three-State Switches	144	

Col	ntents		хi
		Programmed Logic Arrays Describing Multiplexers with a Graphic Vector Notation Special Purpose MSI Parts Problems References	147 153 154 158 161
8	Seq	uential Circuits	163
	8.4 8.5 8.6	Storage of Information Clocking Registers Memory Element Input Logic A First Design Example The J-K Flip-Flop Design of Counters MSI Registers and Counters Problems References	163 166 171 173 174 177 181 187 195
9	Syn	thesis of State Machines	199
	9.5	A Language is Needed Standard Symbols for the ASM Chart Vending Machine Control From ASM Charts to Transition Tables Circuit Realization The State Diagram, an Alternative Notation Compatible States Problems References	199 200 204 208 212 216 221 223 227
10	Re	gister Transfer Design	229
	10.2 10.2 10.3 10.4 10.6 10.7 10.8 10.9	ASM Chart Representation of a Control Unit Register Transfer Language (RTL) Notation Construction of a Data Unit from an RTL Description Timing of Connections and Transfers Sequencing of Control Combinational Logic and Conditional Transfers Graphical and RTL Bus Notation Timing Refinements in RTL Systems	229 231 233 239 242 245 248 254 256 257 262 266

XII Contents

11	Small Computer Organization and			
	Pro	ogamming	267	
	11.1	Introduction	267	
	11.2	) - 8	268	
	11.3	8	270	
	11.4	1		
		Computer	272	
	11.5	8	279	
	11.6		286	
	11.7 11.8		290	
	11.0	Programming Procedures Problems	292	
		Troblems	296	
12	Add	dressing and Assembly Language	301	
	12.1		301	
	12.2	Addressing Modes	302	
	12.3		311	
	12.4		316	
	12.5	Data Conversion, Decimal Arithmetic, and Subroutines	320	
		Problems	330	
13	Mei	mory and Input/Output	333	
	13.1	Memory Mapping	333	
	13.2	Timing of Memory Operation	338	
	13.3		340	
	13.4		346	
	13.5	Programming Time Delays	355	
	13.6	Device Drivers	359	
	13.7	Substituting Input Scanning for Combinational Logic	366	
	13.8	Time-Sharing of Interface Ports	370	
		Problems	375	
		References	378	
14	Serial Input/Output			
	14.1	Serial to Parallel Conversion	379	
	14.2		388	
	14.3	A Subroutine for Serial I/O through a TBSIA	393	
	14.4	Interconnecting RS-232 Equipments	396	
	14.5	Computer Networks	400	
		Problems	403	
		References	406	

Contents				xiii	
15	Additional Programming Topics				
	15.1	Pointe	r Addressing and Stacks	407	
	15.2	Subro		411	
		Interru		426	
	15.4		ip and Reset	437	
	15.5	Tables	and Other Data Structures	439	
		Proble	ms	450	
		Refere	ences	455	
			David Contama Davien	457	
16	MIC	ropro	cessor-Based Systems Design	457	
	16.1	Introd		457	
			ng Machine Operation	457	
	16.3		n Specifications	459	
	16.4		ol Unit Design	462	
			ng the Program	465	
	16.6		ry Map Layout	471	
	16.7		g the Program	475 479	
		Proble	ems	4/9	
17	The Clock-Mode Assumption Reexamined			481	
	17.1	Attent	ion to Output Waveforms	481	
	17.2		nation of Hazards	484	
		Synch	nchronizing Inputs to Clock-Mode Circuits		
•			Skew on Edge-Triggered Flip-Flops	491	
	17.5		t Clock Really Necessary?	493	
	17.6	Synthe	esis of Level-Mode Sequential Circuits from a Flow		
				498	
			in State Variable Transitions	504	
	17.8		al Race-Free State Assignments	511	
	17.9		Constraints on Level-Mode Realizations	516	
		Proble		518	
		Refere	ences	522	
Apr	end	ix A	Powers of Two	523	
		ix B			
	,			524	
Ap	pend	lix C	TB6502 Instruction Set: Opcodes,		
			Bytes, Cycles	527	
Appendix D			Mapping the TB6502 into the 6502	530	
Ind	Index				