

Session 0: Invited papers	
0.1 Design for testability survey E.J. McCluskey, Stanford, USA	1
0.2 Диагностика неисправностей регулярных технологи- ческих структур (Fault diagnosis of regular technological structures) A.D. Zakrevski, Minsk, USSR	6
0.3 A survey on the concepts of functional level test generation J. Sziray, Budapest, Hungary	15
0.5 Методы редукции данных для диагностики неисправностей (Methods of diagnostic data compression) V. P.Tchipulis, Vladivostok, USSR	278
Session 1: Design of fault-tolerant systems	
1.1 Highly reliable digital signal processor with simultaneous failure tolerance M.Kameyama, T.Higuchi, Sendai, Japan	26
1.2 System architecture and Protection mechanisms of the MuTEAM multimicroprocessor R. Cardini, M. La Manna, L.Lopriore, L. Strigini, Rome-Pisa, Italy	32
1.3 Protection and error confinement in a message- passing environment: the MuTEAM kernel E. Baiardi, A. Fantechi, A. Tomasi, M. Vanneschi, Pisa, Italy	37
1.4 Reliability design of an image integration memory for a spaceborn telescope M. Gartner, Braunschweig, FRG	43
1.5 Integrated design methodology of failure tolerant system A. Ciuffoletti, L. Simoncini, Rome-Pisa, Italy	49
Session 2: Modeling and evaluation of highly reliable systems	
2.1 A comparison among four different modular redundancy techniques in a computing system P. Velardi, Rome, Italy	55
2.2 A hierarchical performance model of a fault- tolerant multimicroprocessor G. Pulkki, L. Saloranta, Helsinki, Finland	61
2.3 Validation methods for fail-safe or fault- tolerant computers P. Caspi, E.Pilaud, J. Pulou, Grenoble, France	68

2.4	Надежностно-функциональная модель протокола сети ЭВМ (Reliability and function orientated model of a computer network protocol) M. Bien, A. Wabik, Wroclaw, Poland	74
2.5	A contribution of fuzzy set theory to reliability of digital systems A. Czogala, W. Pedrycz, Gliwice, Poland	81
2.6	The improvement of magnetic disk information retrieval using the protective redundancy V.Baltac, I.Tutoveanu, V.Barbunoiu, Bucarest, Roumania	87
<b>Session 3: Software reliability</b>		
3.1	A method for arithmetic microprograms derivation A. Lewinski, Warwaw, Poland	93
3.2	Метод построения корректных программ (Method of writing correct programs) D. Avreski, V. Sirleshova, Sofia, Bulgaria	99
3.3	Evaluating a symmetric fault-tolerant operating system with Petri nets J.Aspelund, R. Linturi, Helsinki, Finland	104
3.4	Data flow in program testing B. Korel, Katowice, Poland	112
<b>Session 4: Test generation</b>		
4.1	The functional d-algorithm. Part I. S. Várszegi, Budapest, Hungary	118
4.2	Adaptive random test generator J. Rada, Prague, Czechoslovakia	123
4.3	A practical method for generating the minimal set of tests of the combinational circuits F. Momeo, M. Balan, Bucarest, Roumania	128
4.4	Обнаружение неисправностей последовательностного автомата на основе полутактовой модели (Fault detection in sequential circuits via half-tact model) V.O. Vasyukevich, A.Yu. Gobzemiz, O.S.Denisenko, A.N. Sklyarevich, Riga, USSR	133
4.5	Временные булевые дифференциалы и их применение в диагностике последовательностных схем (Time Boolean difference and its application to the diagnosis of sequential circuits) Yu.A. Skobtsov, Donetsk, USSR	138

4.6	Представления дискретных автоматов (Representation of discrete automata) I.S. Grunski, Donetsk, USSR	142
4.7	Поиск минимальных распознающих слов для конечного автомата (On finding the minimal distinguishing sequences for finite automaton) V.G. Skobelev, Donetsk, USSR	143

#### Session 5: Test simulation

5.1	Modeling the detection time of failures affecting the girth of a CPU die B. Courtois, P. Marchal, Grenoble, France	151
5.2	Bidirectional simulation - a new approach to test generation D. Reinert, Karl-Marx-Stadt, GDR	157
5.3	A deductive simulation for multiple-fault in logic circuits K. Sapiecha, K. Walczak, Warsaw, Poland	163
5.4	Graphic language for switching circuits function description J. Piotrowski, Poznan, Poland	169

#### Session 6: Testable design

6.1	Remarks on untestable lines in sequential circuits E. Hübel, Ilmenau, GDR	175
6.2	Inserting test points for simple test generation W. Coy, A. Vogel, Bremen, Bonn, FRG	180

#### Session 7: Self-testing systems

7.1	The algorithm for determining concurrent self-diagnosis of multiprocessor systems H. Krawczyk, Gdansk, Poland	188
7.2	Self-diagnosis in multimicroprocessor systems: the MuTEAM approach P. Ciompi, F. Grandoni, L. Simoncini, Pisa, Italy	193
7.3	Self-testing microprocessor devices E. Michta, Zielona Gora, Poland	200
7.4	The use of diagnostic timers F. Novak, Ljubljana, Yugoslavia	205

### Session 8: System diagnostics

- |     |  |     |
|-----|--|-----|
| 8.1 | The LMDS-Fault location microdiagnostic system<br>J. Zelený, Prague, Czechoslovakia  | 211 |
| 8.2 | The structure and properties of the LMDS tests<br>A. Pluháček, Prague, Czechoslovakia  | 216 |
| 8.3 | A hardware approach to the error diagnostics<br>of a medium size Romanian computer<br>G. Samoila, Bucurest, Roumania                     | 221 |
| 8.4 | Testování CNC systémů Tesla<br>(Testing of the CNC systems TESLA)<br>P. Žák, Kolín, Czechoslovakia                                       | 223 |
| 8.5 | Realizace diagnostiky grafických systémů<br>(Implementation of diagnostics in graphical<br>systems)<br>J. Smíšek, Prague, Czechoslovakia | 228 |

### Session 9: Self-checking checkers

- |     |  |     |
|-----|--|-----|
| 9.1 | Design of self-checking checker for 1-out-of-n<br>code<br>V. Rabara, Žilina, Czechoslovakia                            | 234 |
| 9.2 | Design of totally self-checking check circuits<br>for some 1-out-of-n codes<br>M. Kotočová, Bratislava, Czechoslovakia | 241 |
| 9.3 | A new totally self-checking checker<br>for 1-out-of-3 code<br>P. Golan, Prague, Czechoslovakia                         | 246 |

### Session 10: Diagnostic devices and systems

- |      |  |     |
|------|--|-----|
| 10.1 | Automatic test system ADT/ZKD<br>P. Štolle, Prague, Czechoslovakia   | 249 |
| 10.2 | Lokalizace poruch pomocí testovacího<br>systému ADT/ZKD<br>(Fault location with the test system ADT/ZKD)<br>V. Škvor, Prague, Czechoslovakia | 254 |
| 10.3 | IC classification on the printed circuit board<br>J. Reviczky, Budapest, Hungary   | 259 |
| 10.4 | Board testing strategy and tool for hardware<br>development<br>B.Csabai, G.Dénes, L.Harmat, A.Reszler,<br>J. Romhányi, Budapest, Hungary     | 264 |
| 10.5 | Logic state analyzer ANISS-20<br>K. Swierc, Katowice, Poland   | 266 |
| 10.6 | The method of increasing the probability of<br>detecting errors for signature analysis<br>A. Hlawiczka, H. Kubica, Gliwice, Poland           | 273 |