

CONTENTS

Opening Session: Inter-Universities Co-operation

Edward Hrynkiewicz, (IE, STU Gliwice, Poland): <i>History and Aims of PDS'96 Conference</i>	9
Tomáš Čermák, (VŠB-TU Ostrava, Czech Republic): <i>Inter-Universities Co-operation</i>	10
Jan Chojcan, (STU Gliwice, Poland): <i>New Trends in Electronics</i>	12

Session A. Industrial Programmable Controllers

Daniel Kaminský, (Dept. of Measurement, FEI, VŠB-TU Ostrava, Czech Republic): <i>Multitasking and Data Acquisition Applications within G Programming Language</i>	17
Edward Hrynkiewicz, Mirosław Chmiel, Andrzej Nowara (IE, STU Gliwice, Poland): <i>Remote I/O Groups Applied in PLCs</i>	25
Wojciech Dinges, Tomasz Ochman-Milarski, Piotr Staniak (ABB, Katowice, Poland): <i>The Application of CANBUS (Controlled Area Network Bus) System in Safety and High Reliable Railway Systems</i>	33
Kazimierz Pasek, Stanisław Świątalski (IAC, STU, Gliwice, Poland): <i>Features of SIPART PS the Intelligent Electropneumatic Positioner</i>	39

Session B1 Field Programmable Logic - Design Means

Mariusz Rawski, Mirosława Nowicka, Paweł Tomaszewicz, Tadeusz Łuba (IT, WUT, Warszaw, Poland): <i>Decomposition-based Logic Synthesis and its Application in FPGA-oriented Technology Mapping</i>	47
Ondřej Novák (Technical University Liberec, Czech Republic): <i>Pseudoexhaustive Test Set Generators for FPGAs</i>	55
Edward Hrynkiewicz (IE, STU Gliwice, Poland): <i>Logic Functions Set Minimization by Reducing of a Boolean Space Occupated by the Generated Implicants</i>	62
Krzysztof Pucher (IE, STU Gliwice, Poland): <i>Improved Term Partition Efficiency in the Implementation of a Single Function in PAL Structures</i>	69
Stefan Kołodziński (Pratt & Whitney Kalisz, Kalisz, Poland): <i>Spectral Methods for Synthesis of Logical Functions Realised in PLD Structures</i>	76
Dariusz Kania (IE, STU Gliwice, Poland): <i>Complex Decomposition of Multiple-Output Functions</i>	86

Session B2: Field Programmable Logic - Applications

Jerzy Kędziera^{A)}, Ryszard Winiarczyk^{A)}, Mieczysław Karaczyński^{B)} (^{A)}ITACS, ^{B)}SCS, Gliwice, Poland):
Notes on Redesigning the FPGA-Based Image Board to the XILINX 4000 Chips Family 95

- Tomasz Garbolino, Adam Kristof (IE, STU Gliwice, Poland):
ICs' Output Cells Modification for Interconnections Testing Purpose 101
- Bohumil Petřželka (VA Brno, Czech Republik):
Programmable Circuits isp - HW Support 108

Session C: Microprocessor Systems and Single-chip Microcomputers

- Andrzej Hławiczka (IE, STU Gliwice, Poland):
A Hamming Code-Preserving Signature Analyzer Checker for Memory with 8-bits Data Words 119
- Vilém Srovnal, Hana Soušková (FEI, VŠB-TU Ostrava, Czech Republic):
Software Development for Real-Time Systems with One-board Microcontrollers 127
- Sergey Y. Yurish, Nikolay V. Kirianaki (State Univ. Lvov Polytechnic, Ukraine):
Single-chip Microcontrollers in Industrial Measuring Systems 133
- Krzysztof Taborek (IE, STU Gliwice, Poland):
An Arbitration Circuit with Maskable Priorities for Multiprocessor System 141
- Zybygiew Rymarski^{A)}, Lechosław Hanák^{B)}, Krzysztof Świątnicki^{B)}, Paweł Wiechula^{B)}
(^{A)} IE, STU Gliwice, Poland, ^{B)} ZPWSAI, Katowice, Poland):
Microcontroller Systems in the Railway Crossing Signalling 147
- František Dohnal, Vladimír Řeřucha (Dept. of TCMR, Military Academy in Brno, Czech Republic):
The Control System of Gyroscope Stabilized Platform Based on MC68332 Microprocessor 154

Session D Discrete Signal Processing

- Jarmil Štursa, Václav F. Kroupa (Institute of R&E, CAS, Prague, Czech Republic):
Direct Digital Frequency Synthesis - Sine Wave Generation with Lookup Table Decomposition 161
- Jan Židek (Dept. of Measurement, FEI, VŠB-TU Ostrava, Czech Republic):
Virtual Flickermeter 168
- Maciej Nowiński (IE, STU Gliwice, Poland):
New Architectures of Integrating Analog-to-Digital Converters 176
- Jacek Izydorczyk (IE, STU Gliwice, Poland):
Hilbert Transform Used for Speech Analysis Enhancement 185
- Miroslav Košek (Dept. of Electrical Engng. Technical Univ. Liberec, Czech Republic):
SW Oriented FFT - Effective Tool for Special Image Operations 191
- Libor Gajdošík (Dept. of E&T, FEI, VŠB-TU Ostrava, Czech Republic):
Error Evaluation at DFT Data Processing 197
- Miroslav Hrianka, Marián Samaš (Dept. of Electronics and E-technology UTC Žilina, Slovakia):
Diagnostics and Analysis of Surface Mount Technology by Image Analysis 200

Session E: Telecommunication

Grzegorz Plonka (IE, STU Gliwice, Poland): Run Length Limited Convolutional Codes	209
Karel Vlček (Dept. of E&T, FEI, VŠB-TU Ostrava, Czech Republic): ATM Error Control by Convolutional Codes	216
Nikolay V. Kirianaki, Sergey Y. Yurish (State Univ. Lvov Polytechnic, Ukraine): Intelligent Adaptive Systems of Telemetry	224
Zbyněk Kocián (Dept. of E&T, FEI, VŠB-TU Ostrava, Czech Republic): VHDL Model of Cyclic Code Programmable Encoder/Decoder	232
Tomáš Dubinský (Dept. of E&T, FEI, VŠB-TU Ostrava, Czech Republic): The Meggit Decoder for Hamming/BCH Codes	239
Marek Šimčák (Dept. of Microelectronics, FEI, Technical University of Brno, Czech Republic): VHDL Model of Huffman Decoder	246

Session F: Posters

Jaromír Kolouch (ÚREL, FEI, VUT Brno): The ispGAL and ispLSI Programmable Logic Devices Used in the Laboratory Exercises	255
Karel Vlček (Dept. of E&T, FEI, VŠB-TU Ostrava, Czech Republic): Testing of PLD Structures by Boundary-Scan Architecture	258
Jozef Čuntala, Lub. Prášil, Ivan Bellan, Dagmar Hogová (Univ.of Transp.and Comm. Žilina, Slovakia): The Training Machine for Development of XILINX Gate Arrays Applications	266
Vitaly Medvedkov, Galina Suvorova (Novosibirsk State Tech. Univ., Russia): Fuzzy Logic Base PID Algorithm	270
Jaroslav Zdrálek (Dept. of E&T, FEI, VŠB-TU Ostrava, Czech Republic): Experience of lesson PLD	274